IN THE CLAIMS:

1-14. (Cancelled)

15. (Currently Amended) A system comprising:

a plurality of multi-periodic, nanometer-scale semiconductor devices formed using the following steps:

(a) depositing a first masking material on a substrate having a first region at a first level and a second region at a second level higher than the first level;

(b) etching the first masking material from the substrate to produce a first sidewall extending from the substrate at an intersection of the first and second regions;

(c) depositing, on the substrate, a second masking material different from the first masking material, the second masking material covering the first and second regions and the first sidewall;

(d) etching the second masking material from the substrate to produce a second sidewall adjacent to the first sidewall, the first and second sidewalls having pitches on the order of nanometers;

(e) repeating steps (a)-(d) a predetermined number of times to produce a plurality of adjacent edge-defined, nanometer-pitched sidewalls alternatingly formed of the first and second masking materials; and

(f) selectively etching one of the first and second masking materials such that the remaining edge-defined, nanometer-pitched sidewalls form a plurality of nanometer-pitched channels on the substrate, wherein each of the semiconductor devices includes at least some of the adjacent, edge-defined, nanometer-pitched sidewalls that form the nanometer-pitched channels and wherein each of the semiconductor devices includes a plurality of the nanometer-pitched channels.

16. (Currently Amended) A plurality of multi-periodic, nanometer-scale

electromechanical devices formed using the following steps:

(a) depositing a first masking material on a substrate having a first region at a first level and a second region at a second level higher than the first level;

(b) etching the first masking material from the substrate to produce a first sidewall extending from the substrate at an intersection of the first and second regions;

(c) depositing, on the substrate, a second masking material different from the first mask material, the second masking material covering the first and second regions and the first sidewall;

(d) etching the second masking material from the substrate to produce a second sidewall adjacent to the first sidewall, the first and second sidewalls having pitches on the order of nanometers;

(e) repeating steps (a)-(d) a predetermined number of times to produce a plurality of adjacent edge-defined, nanometer-pitched sidewalls alternatingly formed of the first and second masking materials; and

(f) selectively etching one of the first and second masking materials such that the remaining edge-defined, nanometer-pitched sidewalls form a plurality of nanometer-pitched channels on the substrate, wherein each of the semiconductor devices includes at least some of the adjacent, edge-defined, nanometer-pitched sidewalls that form the nanometer-pitched channels and wherein each of the electromechanical devices includes a plurality of the nanometer-pitched channels.

17-25. (Cancelled)

26. (Currently Amended) ~~The semiconductor device of claim 25 comprising~~ A semiconductor device formed using the following steps:

(a) forming a first sidewall of first masking material on a substrate, the first sidewall having nanometer-scale width;

(b) depositing a second masking material on the substrate, such that the second masking material covers the first sidewall with a first thickness, forms second and third sidewalls on first and second sides of the first

sidewall with a second thickness being less than the first thickness, and covers the substrate in regions adjacent to the second and third sidewalls with the first thickness;

(c) etching portions of the second and third sidewalls from the substrate such that the first and second sides of the first sidewall form discontinuities in the second masking material;

(d) removing the first sidewall from the substrate leaving a channel in the second masking material having substantially the same width as the first sidewall;

(e) etching a channel in the substrate corresponding to the channel in the second masking material, wherein the semiconductor device includes the channel;

(f) a fourth sidewall of nanometer-scale dimensions formed in the channel;

(g) fifth and sixth sidewalls of nanometer-scale dimensions on opposite sides of the fourth sidewall to form a mushroom-shaped structure; and

(h) wherein the mushroom-shaped structure comprises a gate material for a semiconductor device.

27-30. (Cancelled)

31. (Original) The system of claim 15 wherein the multi-periodic, nanometer scale devices include one of: a heterostructure field effect transistor (FET), a heterojunction bipolar junction transistor (BJT), a gallium-nitride-based FET, an indium-gallium-arsenide-based FET, a gallium arsenide FET, an indium-gallium-arsenide-based FET, and a gallium phosphide FET.

32-33. (Cancelled)

34. (Previously Presented) A semiconductor structure having an edge-defined, nanometer-pitched feature, the semiconductor structure comprising:

(a) a substrate comprising a first layer including a first semiconductor material and a second layer including a second semiconductor material, the first semiconductor material being different from the second semiconductor material; and

(b) at least one nanometer-pitched channel being formed in a masking material located on the substrate, the nanometer-pitched channel being formed using edge definition lithography.

35-37. (Cancelled)

38. (Previously Presented) The semiconductor structure of claim 34 wherein the channel extends into at least one of the first and second layers.

39. (Previously Presented) A semiconductor structure including at least one micrometer-scale feature and at least one nanometer-scale feature being defined using edge definition lithography, the semiconductor structure comprising:

(a) a semiconductor substrate;

(b) at least one micrometer-scale feature being located in or on the semiconductor substrate; and

(c) at least one nanometer-scale feature being located in or on the micrometer-scale feature, the nanometer-scale feature being defined using edge definition lithography, wherein the micrometer-scale feature comprises a channel formed in the substrate and the nanometer scale feature comprises a sidewall located in the channel.

40. (Cancelled)

41. (Previously Presented) A semiconductor structure including at least one micrometer-scale feature and at least one nanometer-scale feature being defined using edge definition lithography, the semiconductor structure comprising:

(a) a semiconductor substrate;

(b) at least one micrometer-scale feature being located in or on the semiconductor substrate; and

(c) at least one nanometer-scale feature being located in or on the micrometer-scale feature, the nanometer-scale feature being defined using edge definition lithography, wherein the micrometer-scale feature comprises a mesa and the nanometer-scale feature comprises a sidewall located on top of the mesa.

42. (Previously Presented) A semiconductor structure including at least one micrometer-scale feature and at least one nanometer-scale feature being defined using edge definition lithography, the semiconductor structure comprising:

(a) a semiconductor substrate;

(b) at least one micrometer-scale feature being located in or on the semiconductor substrate; and

(c) at least one nanometer-scale feature being located in or on the micrometer-scale feature, the nanometer-scale feature being defined using edge definition lithography, wherein the micrometer-scale feature comprises a channel or hole being defined by the substrate and wherein the nanometer-scale feature comprises a channel located in a masking material deposited in the hole.

43. (Previously Presented) A semiconductor structure including at least one micrometer-scale feature and at least one nanometer-scale feature being defined using edge definition lithography, the semiconductor structure comprising:

(a) a semiconductor substrate;

(b) at least one micrometer-scale feature being located in or on the semiconductor substrate; and

(c) at least one nanometer-scale feature being located in or on the micrometer-scale feature, the nanometer-scale feature being defined using edge definition lithography, wherein the micrometer-scale feature comprises a mesa located on the substrate and wherein the nanometer-scale feature comprises a channel located in a masking material deposited on the mesa.

44. (Previously Presented) A field effect transistor having an edge-defined gate, the field effect transistor comprising:

(a) a substrate including a buffer layer of a first semiconductor material and a channel layer of a second semiconductor material, the second

semiconductor material being different from the first semiconductor material; and

(b) a gate electrode being located on the substrate between the source and drain electrodes, the gate electrode being formed using edge definition lithography and wherein the gate electrode includes a first portion that extends outward from the substrate and a second portion that extends in a direction transverse to the first portion and overhangs the substrate.

45. (Original) The field effect transistor of claim 44 wherein the substrate comprises a donor layer comprising a third semiconductor material being different from the first and second semiconductor materials, the donor layer including a channel, wherein the gate electrode is located in the channel.

46. (Original) The field effect transistor of claim 45 wherein the channel extends into the channel layer.

47. (Original) The field effect transistor of claim 44 wherein the channel layer includes a channel and the gate electrode is located in the channel.

48. (Original) The field effect transistor of claim 44 wherein the substrate includes a donor layer adjacent to the channel layer and the gate electrode is located on the donor layer.

49. (Original) The field effect transistor of claim 44 wherein the gate electrode is located on the channel layer.

50. (Previously Presented) A bipolar junction transistor having a nanometer-scaled edge-defined feature, the bipolar junction transistor comprising:

(a) a collector layer;

(b) a base layer being adjacent to the collector layer; and

(c) a nanometer-scale emitter being defined on the base layer using edge definition lithography, wherein the emitter extends outward from the base layer.